

FIG. 1

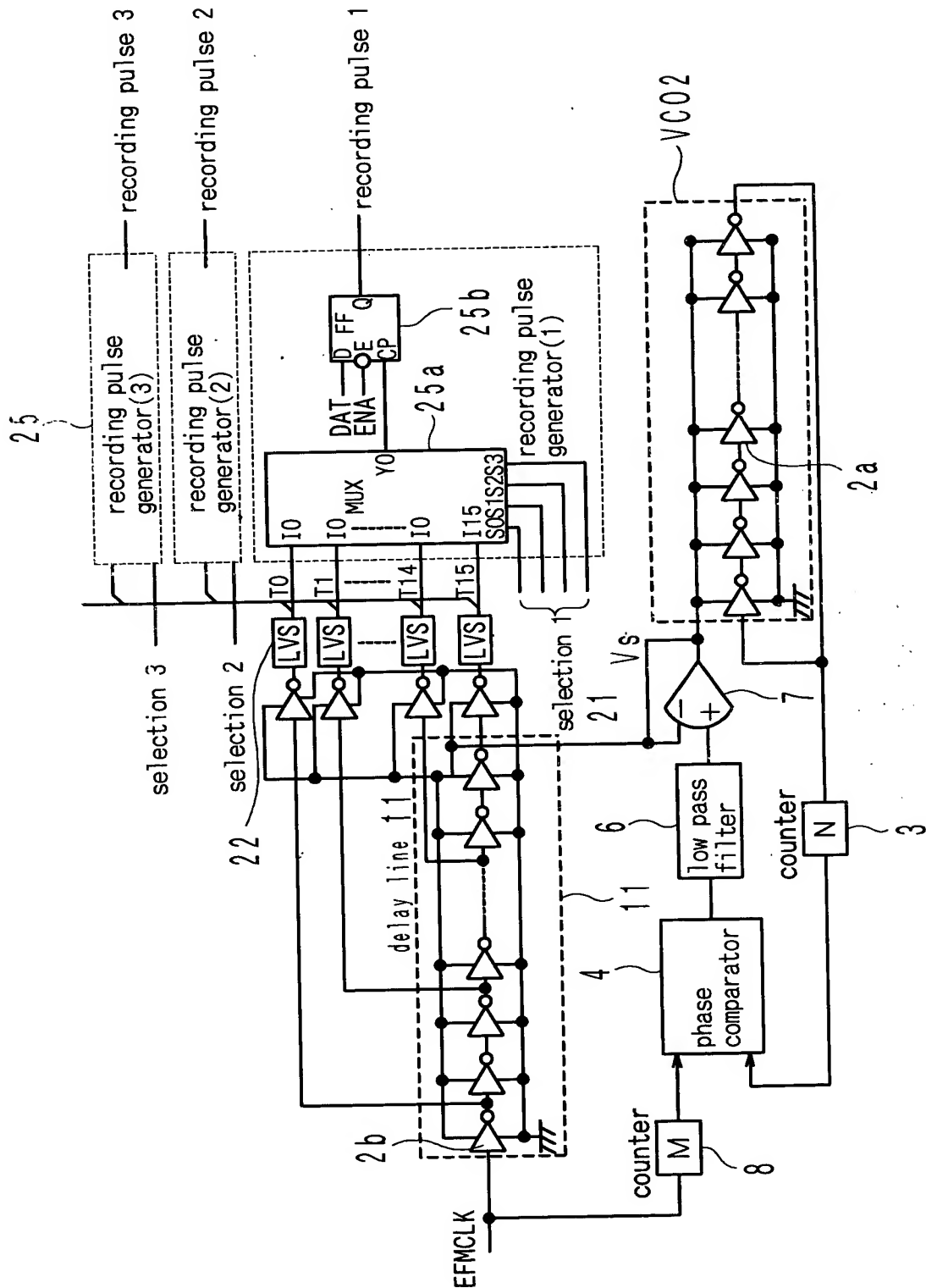
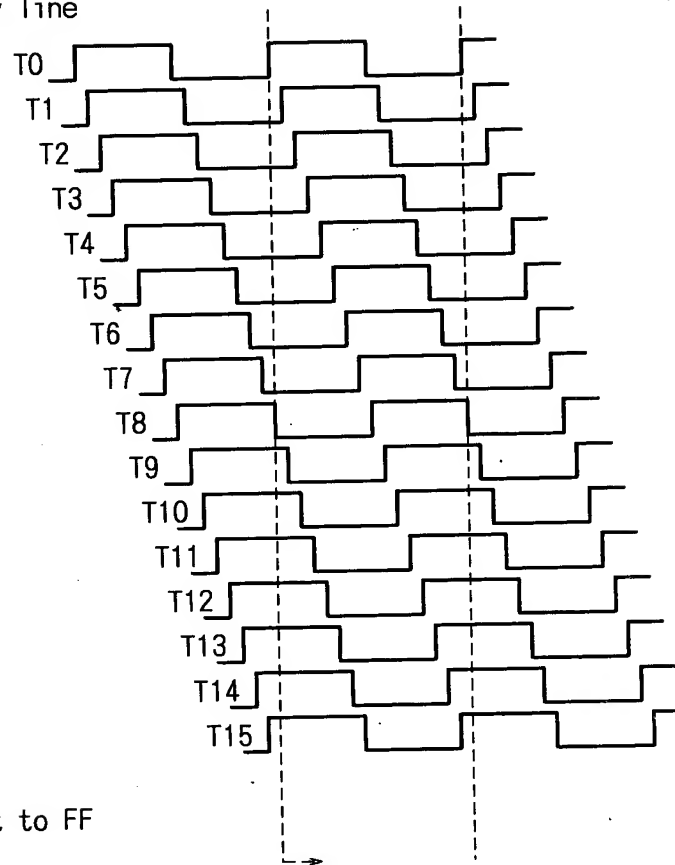


FIG. 2

output of delay line



clocks input to FF

FIG. 3

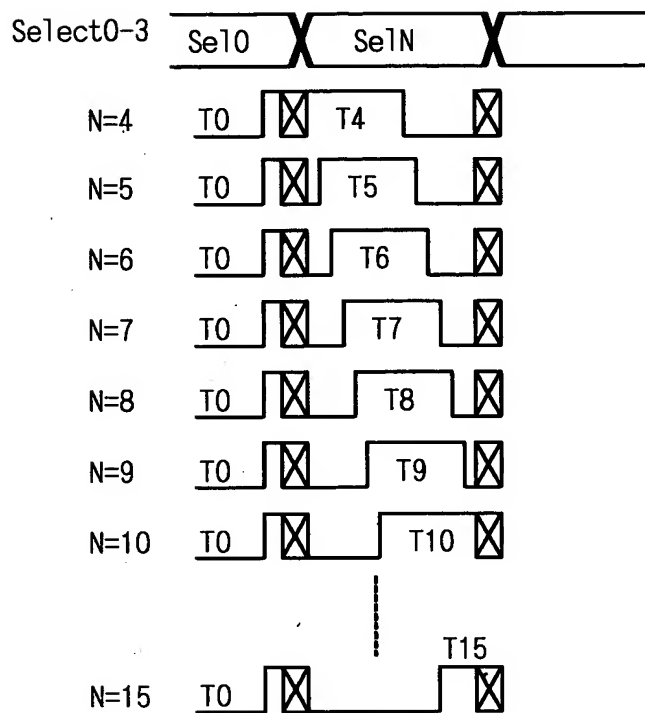


FIG. 4

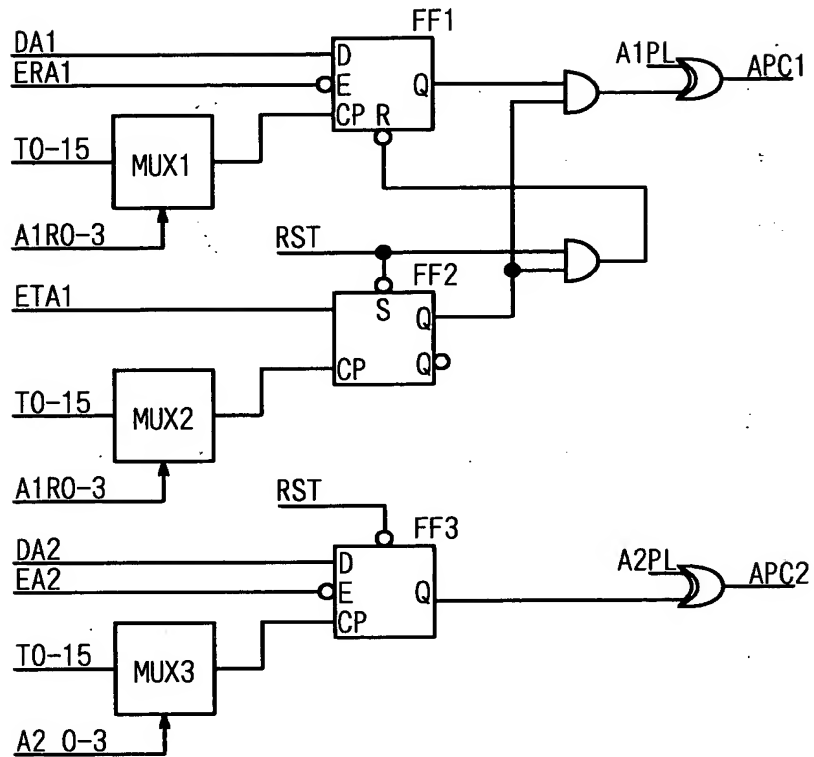


FIG. 5

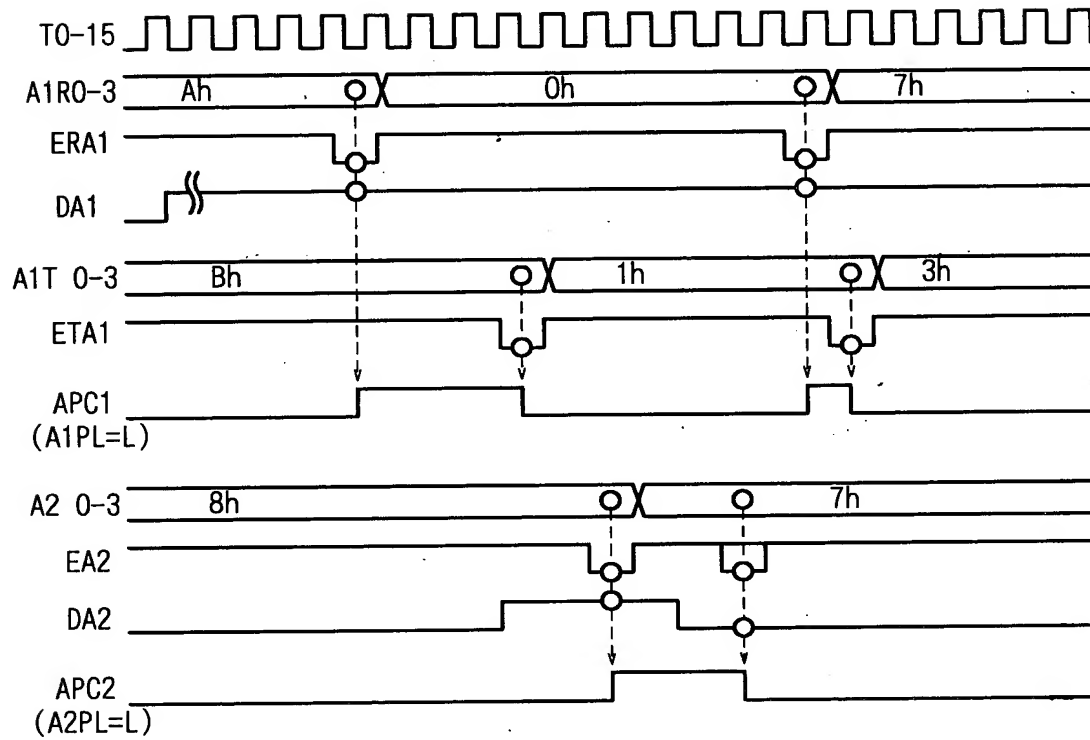


FIG. 6

signals	contents	Active
RST	reset	L
T0-15	Fine Clock input	
DA1	APC1 Leading data	
ERA1	APC1 Leading Enable	L
A1R0-3	APC1 Leading Clk Select	
ETA1	APC1 Training Enable	L
A1T0-3	APC1 Training Clk Select	
DA2	APC2 data	
EA2	APC2 Enable	L
A2 0-3	APC2 Clk Select	

signals	contetns	Active
RST	reset	L
T0-15	Fine Clock input	
DA1	APC1 Leading data	
ERA1	APC1 Leading Enable	L
A1R0-3	APC1 Leading Clk Select	
ETA1	APC1 Training Enable	L
A1T0-3	APC1 Training Clk Select	
DA2	APC2 data	
EA2	APC2 Enable	L
A2 0-3	APC2 Clk Select	

FIG. 7

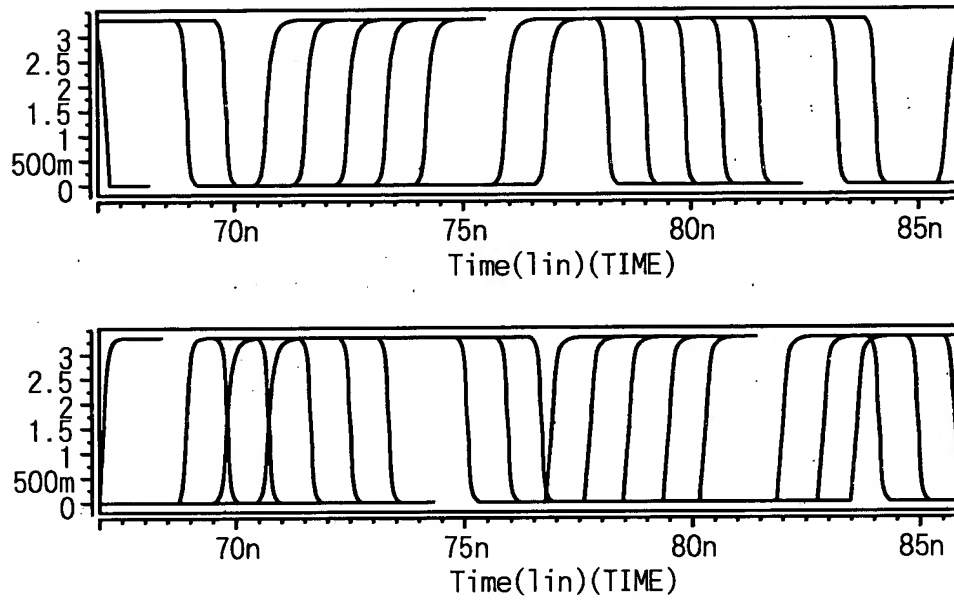


FIG. 8

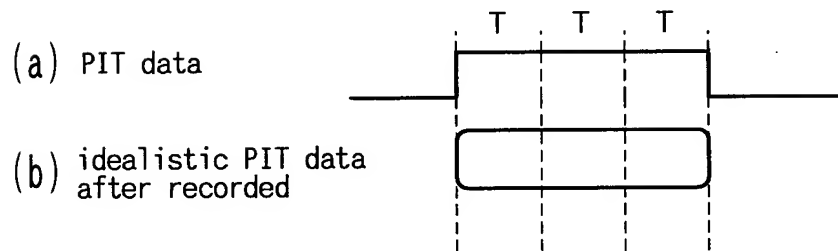


FIG. 9

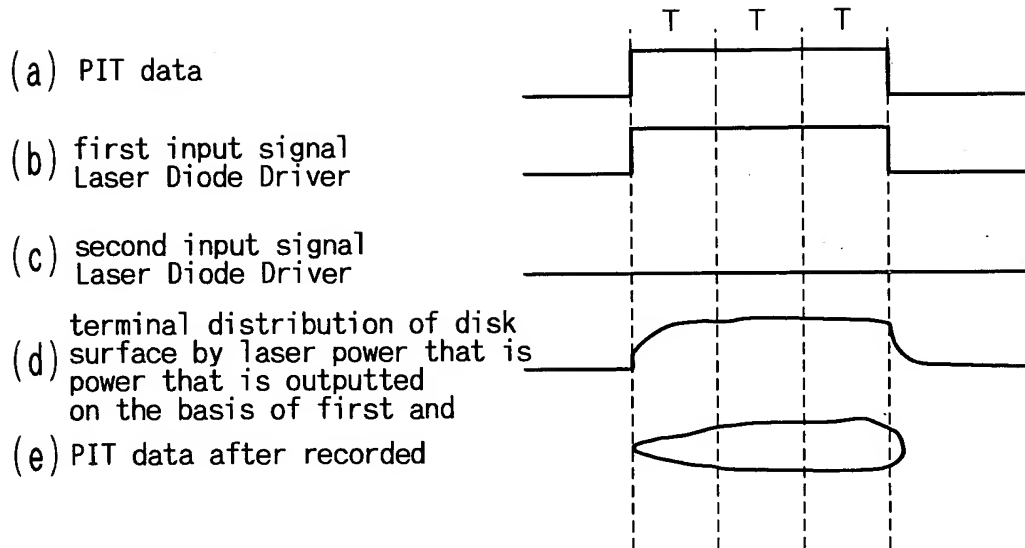


FIG. 10

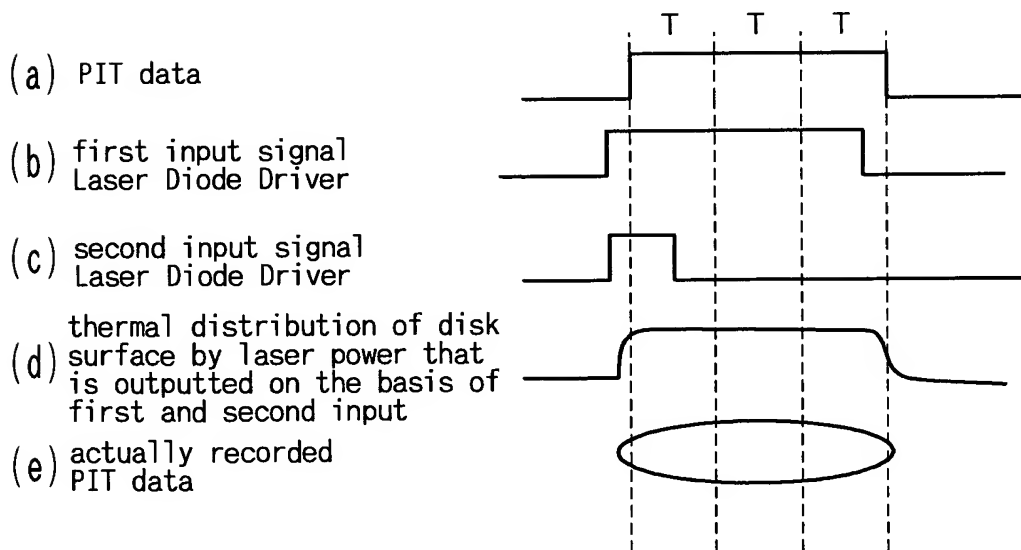


FIG. 11

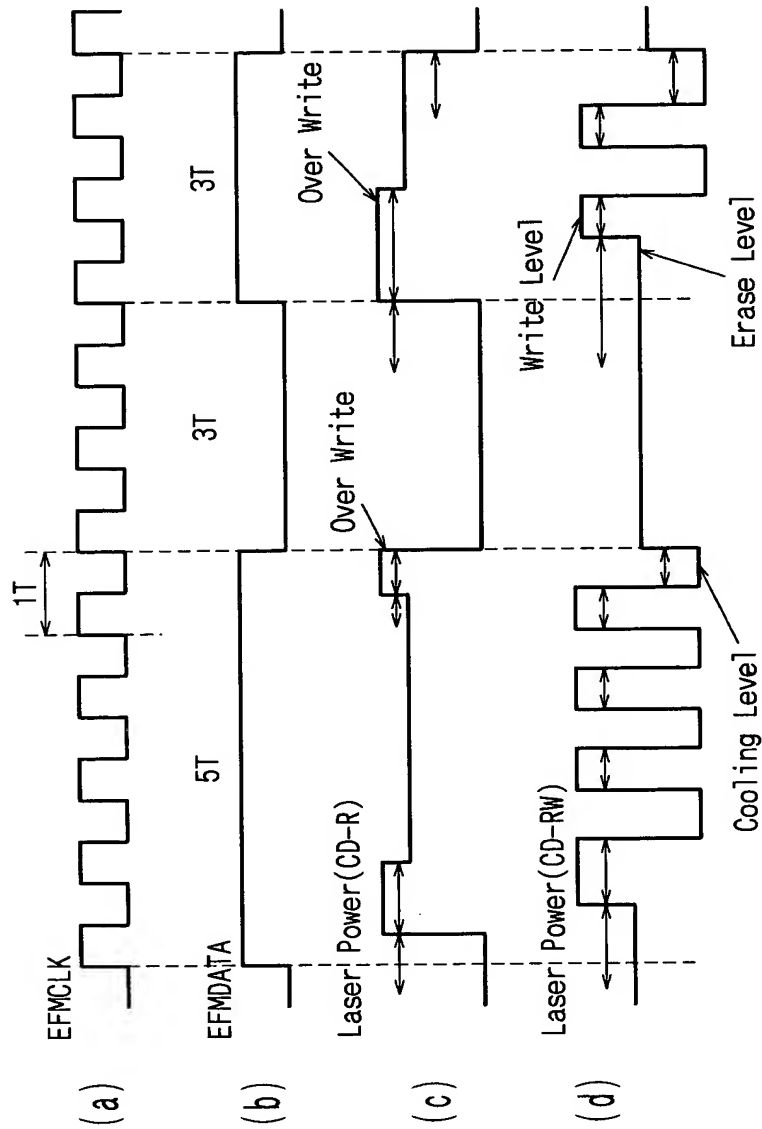


FIG. 12

recording speed	EFMCLK [MHz]	T(period) [ns]	T/16 [ns]
1	4.32	231.38	14.46
2	8.64	115.69	7.23
4	17.28	57.85	3.62
8	34.57	28.92	1.81
16	69.14	14.46	0.90
32	138.29	7.23	0.45
36	155.58	6.42	0.40
40	172.87	5.78	0.36
48	207.44	4.82	0.30



FIG. 14

